

TRF370x Quadrature Modulator Evaluation Module

User's Guide



Literature Number: SLWU062

March 2010

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TRF370x Quadrature Modulator Evaluation Module

1 Overview

This document relates to the TRF370x direct quadrature modulator for applications in the transmit path of base stations and communications equipment. The quadrature modulator is used for upconversion of signals from the transmit chain DAC to the RF power amplifier device. Evaluating modulator complex performance involves careful bias-voltage setup, an LO signal, and two differential (I/Q) signals at the input of the modulator. This document describes the wide range of test options available and the factors that must be considered in using this EVM.

1.1 Purpose

The TRF370x evaluation module (EVM) is intended for the evaluation of the TRF370333, TRF370317, TRF370315, and TRF370417 direct-launch quadrature modulators. Unless otherwise stated, the functionality described in this manual applies to all the TRF370x devices.

1.2 EVM Circuit Overview

The EVM comes configured for differential I/Q input signals via four SMA connectors as shown in the schematic, [Figure 14](#), and in [Table 1](#).

For the upper sideband, the I signals are connected to J4 (I+) and J3 (I–). The Q signals are connected to J5 (Q–) and J6 (Q+). The LO signal is fed to SMA connector J1, whereas J2 must be terminated with 50 Ω to ground. SMA connector J7 is used to monitor the RF output signal from the quadrature modulator (U1).

The quadrature modulator requires a supply voltage of 4.5 V–5.5V from a regulated power supply through headers TP2 and TP4.

The TRF370x quadrature modulators require a dc common-mode bias voltage (3.3 VDC, 1.7 VDC, or 1.5 VDC, corresponding to the last two digits of the part number) on all four input pins.

1.3 Power Requirements

The TRF370x EVM requires two 5-V V_{CC} dc power-supply connectors through headers TP2 and TP4. Header TP4 supplies 5 V to the LO circuitry, and TP2 supplies 5 V to the modulator circuitry.

CAUTION

Voltage Limits

Exceeding 5.6 V may damage the TRF370x.

1.4 TRF370x EVM Operating Procedure

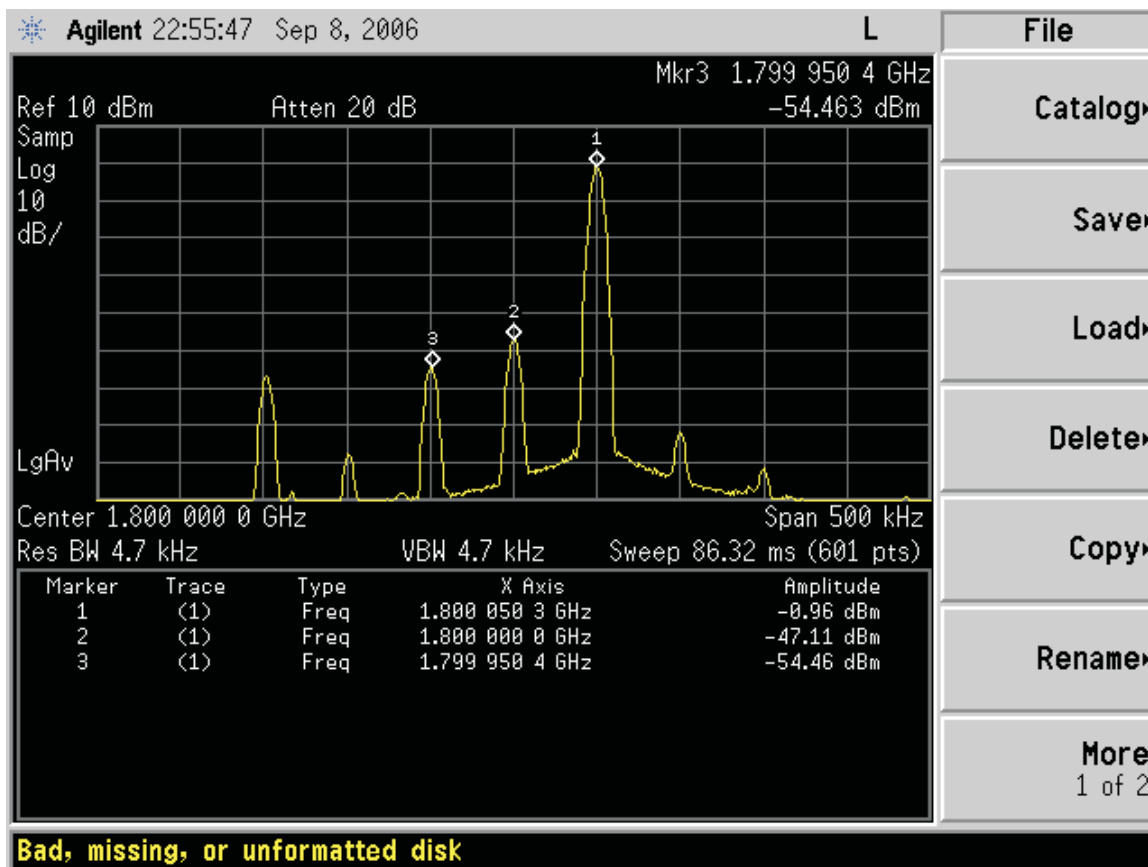
Set up the EVM as follows:

1. Power-supply connection:
 - (a) Switch on the V_{CC} (5-V) supply and set the current limit to 235 mA.
 - (b) Connect the 5-V supply to headers TP2 and TP4. Connect ground to TP1 and TP3.
 - (c) Verify that the current draw is ≤ 205 mA for the TRF370x1x and ≤ 235 mA for the TRF370333.
2. Use a suitable 50- Ω output signal generator or the TRF3761 to supply the LO signal at the desired frequency to J1, and terminate J2 with 50 Ω to ground.
3. Use a DAC or an arbitrary waveform generator to provide the I/Q input signals. A typical setup is as follows: a 1-V_{p-p} sine wave, a frequency of 50 kHz, a dc offset of 0 V, and an output impedance of 50 Ω (typically an ESG vector signal generator or similar).
4. Set the common mode on the ESG to either 1.65 V, 0.75 V, or 0.85 V, depending on device type (set to 1.65 V for the TRF370333, to 0.75 V for the TRF370315, or to 0.85 V for the TRF370x17).
5. Use an arbitrary waveform generator to suppress the sideband. Adjust the I/Q amplitude and phase of the CW signal coming from the arbitrary waveform generator.
6. Connect a spectrum analyzer to the SMA connector marked RFOUT (J7) and monitor the TRF370x output.

1.4.1 Typical Test Results

1.4.1.1 Unadjusted Sideband Suppression

Unadjusted sideband suppression measures the amount of the unwanted sideband of the input signal, relative to the wanted sideband. This assumes that the baseband inputs delivered to the modulator input pins are perfectly matched in amplitude and are exactly 90° out of phase. Unadjusted sideband suppression is measured in dBc. An iterative test is required in order to match perfectly the inputs to the modulator. This ensures that any equipment, board, or signal conditioning component imbalances are corrected before the signals are applied to the device under test. Once the baseband inputs to the modulator are balanced, the amount of suppression attained is a measure of the internal mismatches of the modulator, inherent to any modulator design. This suppression is the one specified in the TRF370x data sheet. See [Figure 1](#).

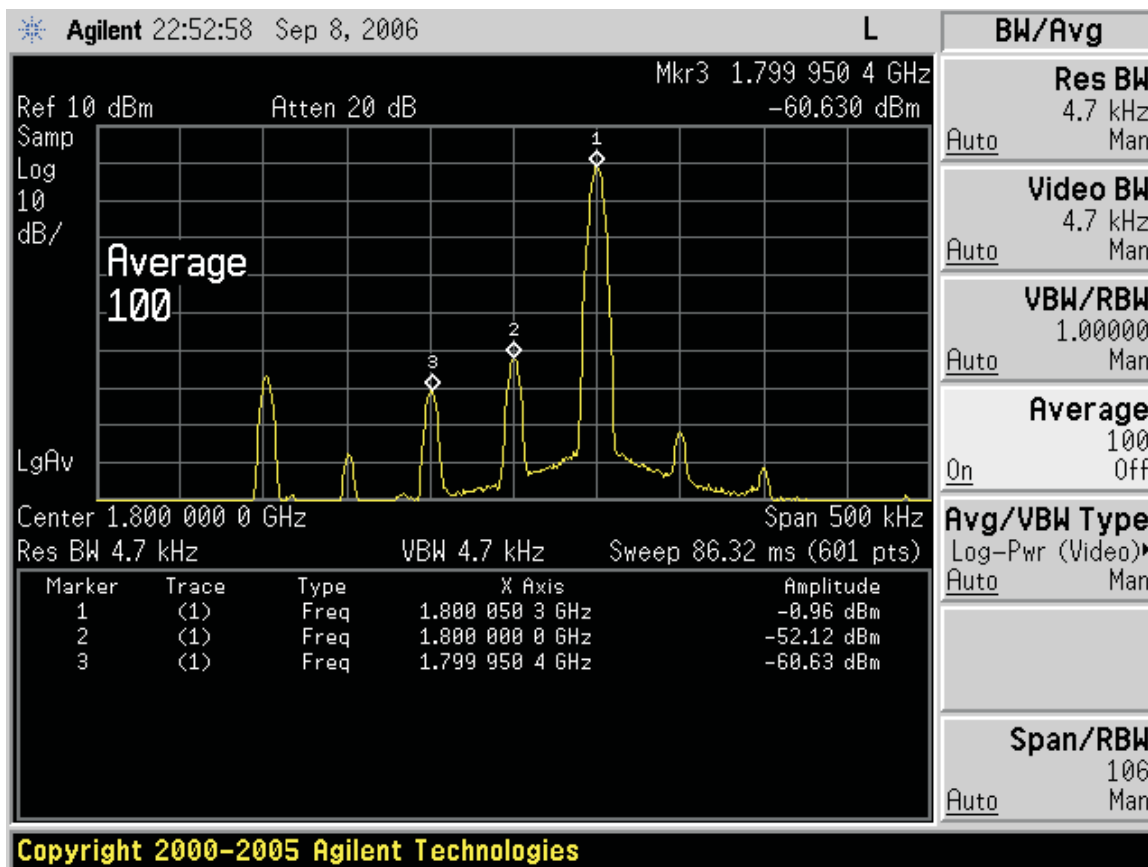


C003

Figure 1. Unadjusted Sideband Suppression

1.4.1.2 Optimized Sideband Suppression

The sideband suppression of the TRF370x can be optimized by adjusting the amplitude and phase balance between the quadrature inputs. The ideal condition is when all four inputs (I, \bar{I} , Q, and \bar{Q}) have exactly the same amplitude and the phase relationship is: $I = 0^\circ$, $\bar{I} = 180^\circ$, $Q = 90^\circ$, and $\bar{Q} = 270^\circ$. Using an iterative procedure, the gain and phase balance can be adjusted to achieve suppression levels that exceed 60 dBc. The level of suppression observed depends on the amount of resolution available from the source driving the modulator. By using TI's DAC568x, the user can take advantage of built-in features to optimize the sideband suppression by changing the amplitude and phase relationship of the signals. If another DAC is used, then the user must provide this level of adjustment by controlling the regular digital inputs to the DAC. See [Figure 2](#).



C002

Figure 2. Optimized Sideband Suppression

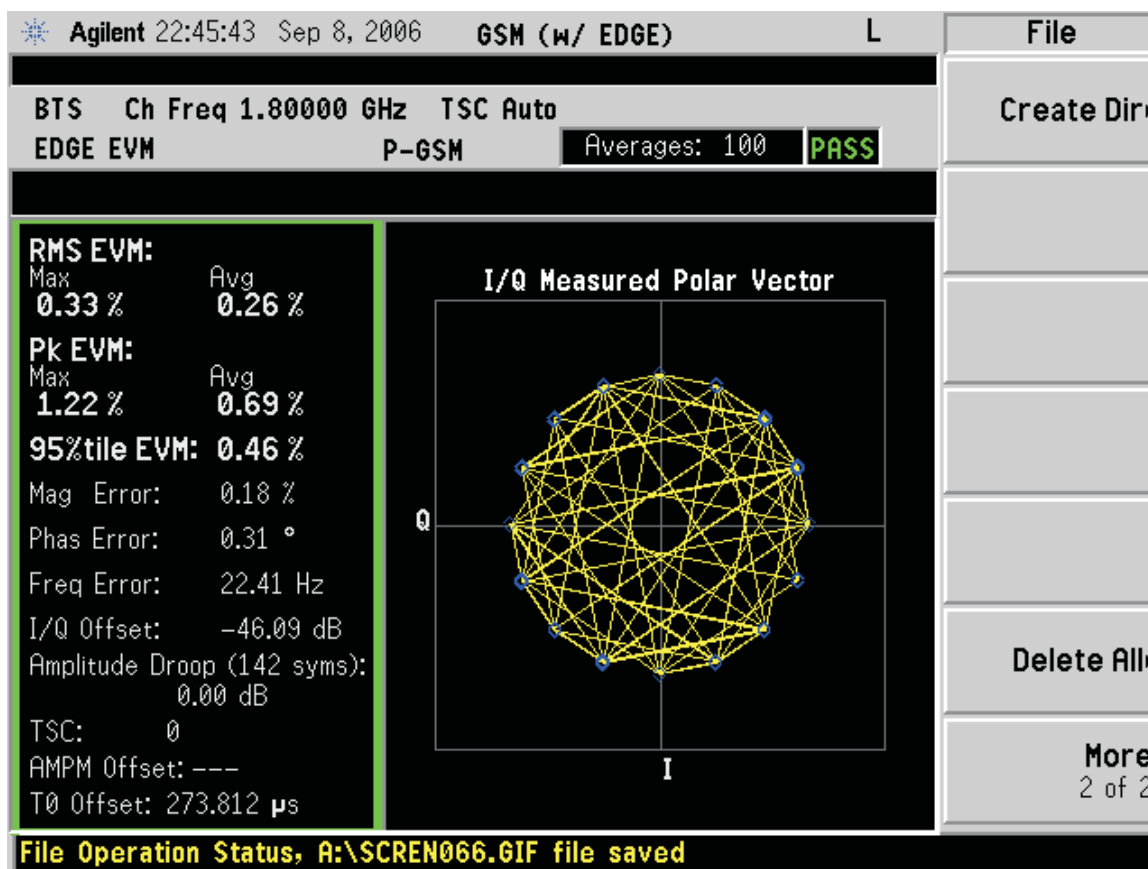
1.4.1.3 Carrier Feedthrough

Carrier feedthrough is the amount of the LO that leaks onto the output spectrum of the modulator. Ideally for the TRF370x, inputs (I, \bar{I} , Q, and \bar{Q}) must be at approximately 3.3 V for TRF370333, 1.5 V for TRF370315, and 1.7 V for TRF370317 and TFR370417. The DAC dc settings are also useful to correct the dc mismatch between I and \bar{I} and between Q and \bar{Q} to minimize the LO feedthrough. If using TI's DAC568x, then the internal controls for the I/Q offsets provide excellent carrier suppression (very low LO leakage). Alternatively, if an ESG is being used, adjust the I and Q voltage offsets in mV steps until you obtain the minimum carrier feedthrough. A typical carrier feedthrough value exceeds -50 dBm. See [Figure 2](#).

1.4.1.4 GSM (EDGE EVM Measurements)

1. Provide a GSM edge signal of the desired frequency into the differential baseband inputs (example sample rate = 4.33 MHz).
2. Use a spectrum analyzer with edge personality to measure the transmit power to either 0 or -5 dBm.
3. PSA: Mode → GSM (with EDGE) → measure → Transmit Pwr (usually 0 or -5 dBm) → more → EDGE EVM.
4. ESG: Mode setup → select waveform → highlight EDGE → select waveform → ARB setup → type 4.33333 MHz → I/Q → I/Q output control → Common mode I/Q offset → (set to 1.65 V, 0.75 V, or 0.85 V, depending on device) → I/Q → I/Q output control → I/Q output atten (adjust to get desired transmit power to either 0 or -5 dBm).

See [Figure 3](#).

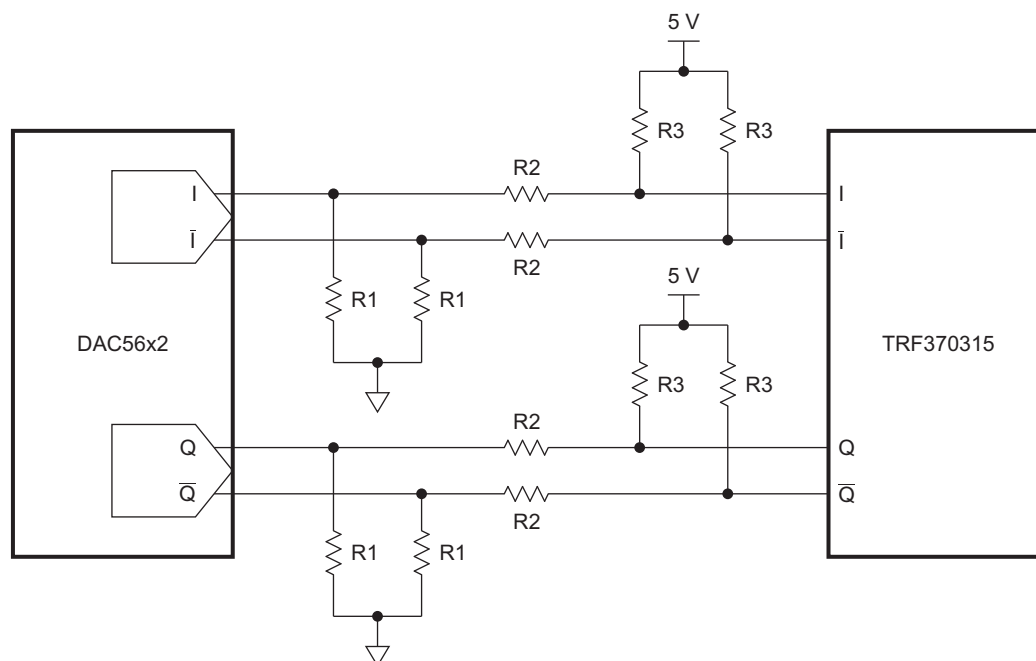


C001

Figure 3. GSM EDGE EVM at 1800 MHz

1.4.2 Interface to TI's DAC

All the TRF370x devices work well with TI's DACs. [Figure 4](#) shows an example of the interface network between a DAC56x2 and a TRF370315. [Figure 5](#) shows an example of interfacing the DAC568x to the TRF370333 with options for selecting the desired amount of attenuation between the two. Additional interfacing networks for each modulator can be found in their respective data sheets or by using the DAC interface calculator ([SLWC083](#)).

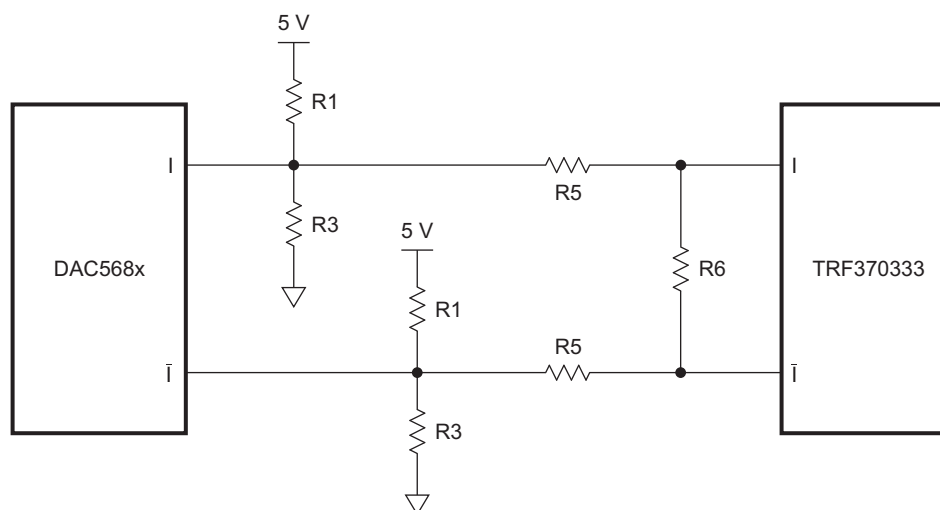


S0225-02

| TYPICAL VALUES | | |
|----------------|--------------|--------------|
| R1 | R2 | R3 |
| 53 Ω | 210 Ω | 931 Ω |

NOTE: A DAC interface calculator is available ([SLWC083](#)).

Figure 4. 1.5-V Interface Network for 19.2 mA Full Scale



S0226-02

| LOSS | | 1 dB | 2 dB | 3 dB | 4 dB | 5 dB |
|----------|----|------|------|------|------|------|
| Pullup | R1 | 115 | 115 | 115 | 115 | 115 |
| Pulldown | R3 | 634 | 634 | 634 | 634 | 634 |
| Series | R5 | 11 | 21 | 30 | 37.4 | 45.3 |
| Shunt | R6 | 187 | 165 | 147 | 130 | 118 |

Figure 5. 3.3-V Interface Network for 19.2 mA Full Scale

2 Physical Description

This chapter discusses the four-layer PCB layout, component placement, and list of components used on the evaluation module.

2.1 PCB Layout

The EVM is constructed on a four-layer, 38,1-mm × 38,1-mm × 1,579-mm thick PCB using FR-4 material. Figure 6 through Figure 12 show the individual layers.

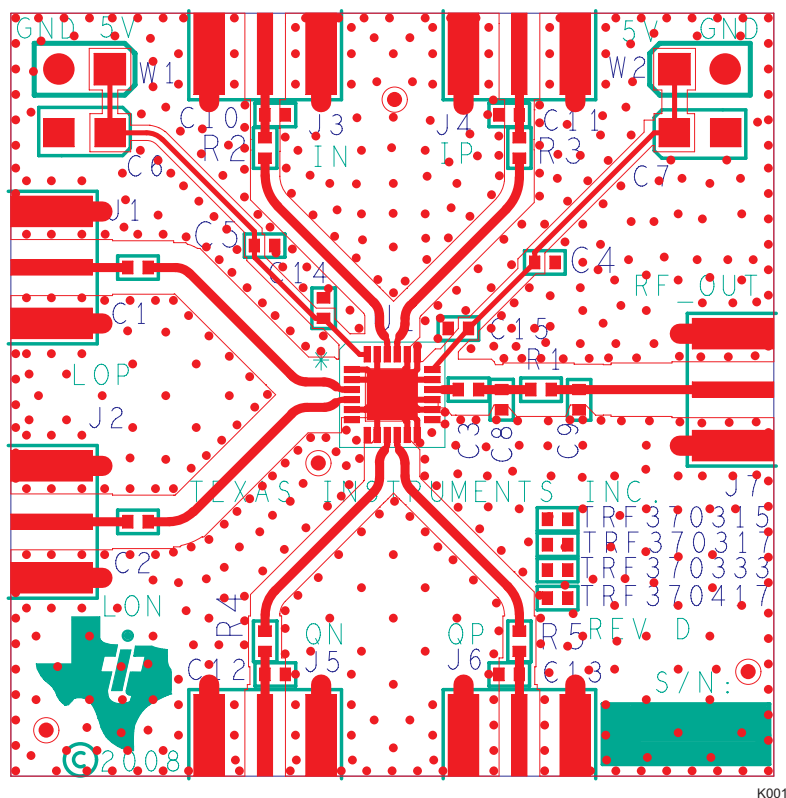


Figure 6. Top Layer 1

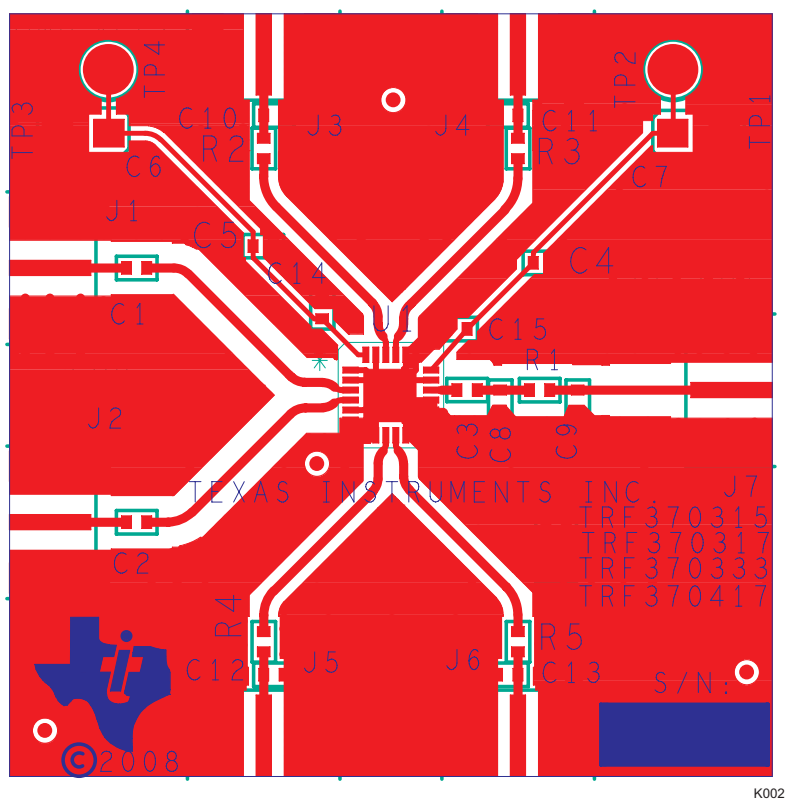


Figure 7. Top Layer 2

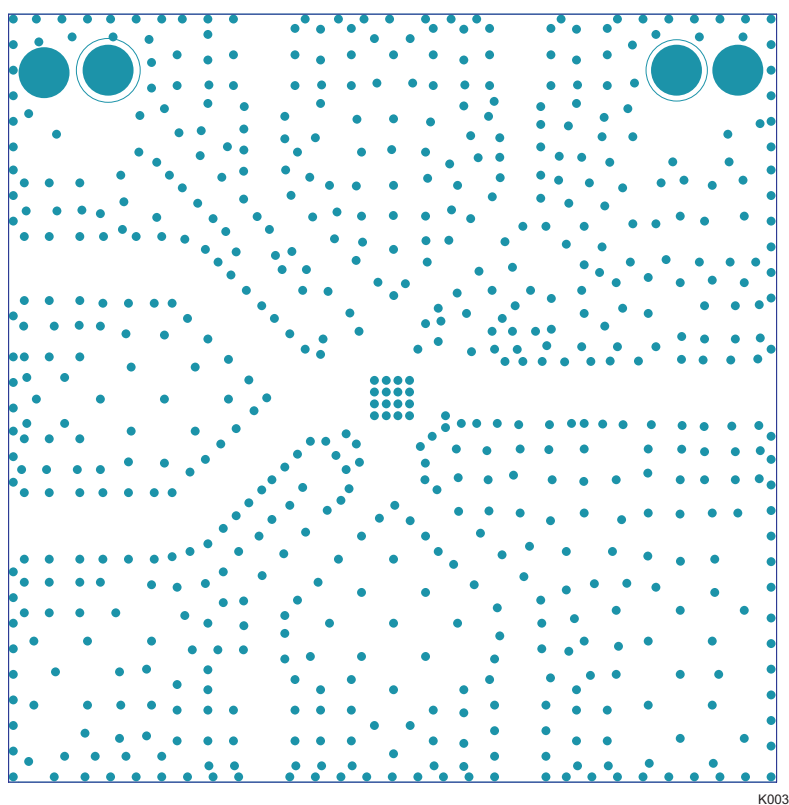
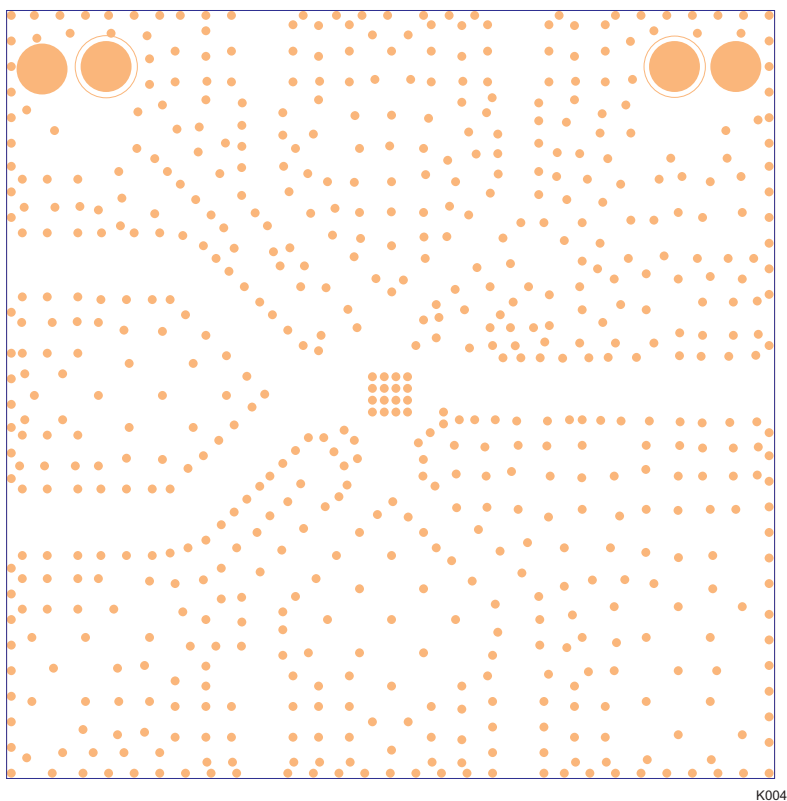
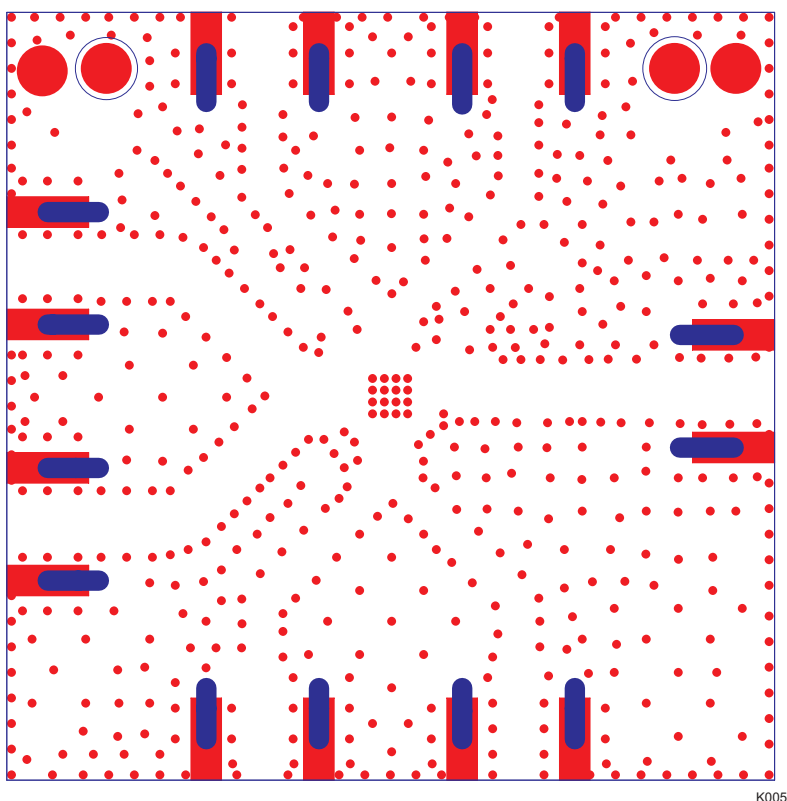


Figure 8. Ground Plane 1



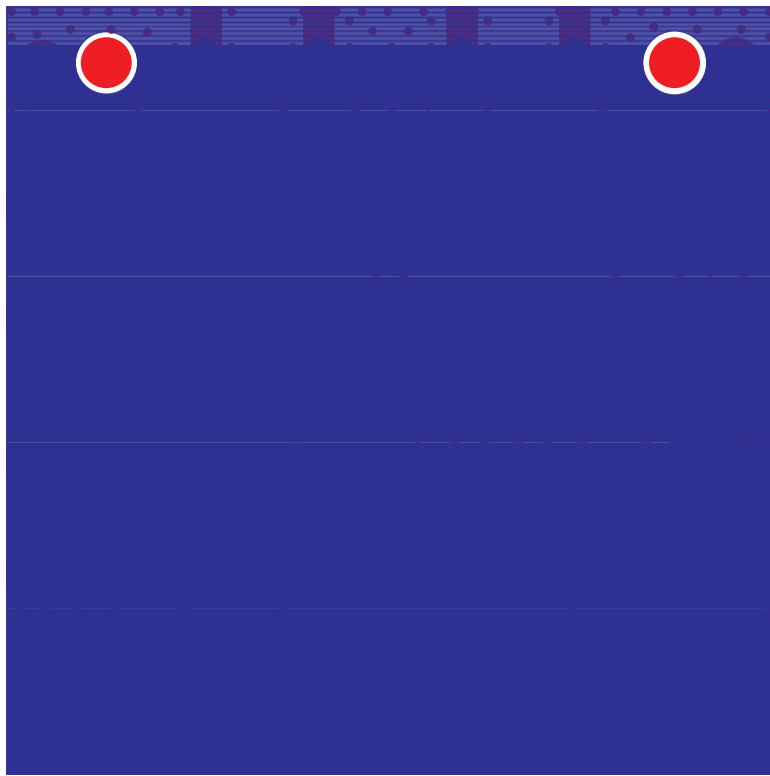
K004

Figure 9. Ground Plane 2



K005

Figure 10. Bottom Layer 1

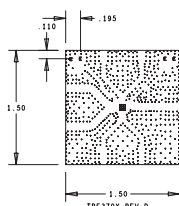


K006

Figure 11. Bottom Layer 2

UNLESS OTHERWISE SPECIFIED, ALL NOTES ARE APPLICABLE.
NOTES PRECEDED BY AN UNMARKED "□" ARE NOT APPLICABLE.

| DRILL CHART: TOP to BOTTOM | | | |
|----------------------------|------|--------|-----|
| ALL UNITS ARE IN MILS | | | |
| FIGURE | SIZE | PLATED | QTY |
| 1 | 8.0 | PLATED | 662 |
| 2 | 40.0 | PLATED | 4 |



- APPLICATION DESIGN MANUFACTURING AND INSPECTION DOCUMENTS, IPC-2221A & IPC-2222 / DESIGN STANDARD FOR RIGID PRINTED CIRCUIT BOARDS AND RIGID PRINTED BOARD ASSEMBLIES.
IPC-6012B / QUALIFICATION AND PERFORMANCE SPECIFICATION FOR RIGID PRINTED BOARD.
IPC-A-600G / ACCEPTABILITY OF PRINTED BOARDS.
- HOLE SIZE APPLY AFTER PLATING. TOLERANCE TO BE $\pm .003$.
- REGISTRATION TOLERANCE: ARTWORK $\pm .002$
ALL HOLE CENTERS $\pm .005$ FROM DIMENSION DATUM.
- MINIMUM COPPER WALL THICKNESS SHALL BE .001 INCH.
FOR ALL PLATED THROUGH HOLES. BREAKOUT NOT ALLOWED.
- PROCESS AND MATERIAL MUST CONFORM TO UL 796. MATERIAL MUST MEET OR EXCEED UL FLAMMABILITY RATING 94V-0.
MATERIAL: ☐ SINGLE SIDE, ☐ DOUBLE SIDE, ☒ MULTI-LAYER POLYCLAD 370HR
TOP METAL TO GND PLANE DIELECTRIC THICKNESS TO BE 10 MILS $\pm .5$ MILS
BOARD THICKNESS: .062 $\pm .006$
NUMBER OF FINISHED LAYERS: 4
- ☒ MANUFACTURE'S UL MARKING, FLAMMABILITY RATING, ☒ LOGO AND DATE CODE TO BE PLACED IN SILKSCREEN ON BOTTOM SIDE OF THE BOARD.
- SOLDERMASK BOTH SIDES USING TAIYO (OR EQUIVALENT). COLOR-RED (0.001 TO 0.002" THICK OVER METAL).
- SILKSCREEN ☒ TOP SIDE ☐ BOTH SIDES. USING ☐ YELLOW ☒ WHITE NPI LEADFREE.
REGISTRATION TOLERANCE TO BE $\pm .005$. INK IS NOT ALLOWED ON EXPOSED PLATED AREA.
- P.C. BOARD TO BE FREE OF DIRT, OIL, FINGER PRINTS, ETC.
- BOARD WARPAGE: WARP AND TWIST SHALL NOT EXCEED .007 INCH PER INCH MEASURED AT ANY LOCATION OR DIRECTION ON THE BOARD.
- BOARD MUST BE 100% ELECTRICALLY TESTED TO ENSURE NO SHORTS OR OPEN CIRCUITS AT 20V.
- ☒ ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- ☒ ALL INNER LAYER THERMALS ON 8 HOLES TO BE CHANGED TO DIRECT TIES TO THE PLANE LAYERS.
- TOP LAYER 18MIL TRACES TO BE 50 OHM IMPEDANCE.
REFERENCE LAYER 2.
- MINIMUM COPPER CONDUCTOR WIDTH IS: 10MIL.
MINIMUM COPPER SPACING IS: 5MIL.
- SMOBC/IMMERSION GOLD: 5-15 μ IN OVER 100-200 NICKEL.
IMMERSION GOLD.
- NO CHANGES TO THE ARTWORK ARE PERMITTED WITHOUT WRITTEN AUTHORIZATION.
- ALL THRU HOLE VIAS TO BE PLUGGED WITH NON-CONDUCTIVE EPOXY MATERIAL.
PLUGGED VIAS TO BE PLATED AFTER PLUGGING TO PRESENT FLAT SURFACE TO DEVICE - NO POTHOLE.
- GROUND ETCH ON ALL LAYERS TO BOARD EDGE IS INTENTIONAL.
DO NOT PULL BACK.

D001

Figure 12. Drill Pattern

2.2 Parts List

Table 1. Bill of Materials for TRF370x EVM

| Item Number | Quantity | Reference Designator | Value | PCB Footprint | Mfr. Name | Mfr. Part Number | Note |
|-------------|----------|----------------------------|-------------|-----------------------|--------------------|--------------------|--------------------------------|
| 1 | 3 | C1, C2, C3 | 100 pF | 0402 | PANASONIC | ECJ-0EC1H101J | |
| 2 | 2 | C4, C5 | 1000 pF | 0402 | PANASONIC | ECJ-0VC1H102J | |
| 3 | 2 | C6, C7 | 4.7 μ F | TANT_A | KERMET | T491A475K016AS | |
| 4 | 0 | C8, C9 | 1 μ F | 0402 | PANASONIC | ECJ-0EC1H010C_DNI | DNI |
| 5 | 0 | C10, C11, C12, C13 | 0.1 μ F | 0402 | PANASONIC | ECJ-0EB1A104K_DNI | DNI |
| 6 | 2 | C14, C15 | 10 pF | 0402 | MURATA | GRM1555C1H100JZ01D | |
| 7 | 7 | J1, J2, J3, J4, J5, J6, J7 | LOP | SMA_SMEL_250x215 | JOHNSON COMPONENTS | 142-0711-821 | |
| 8 | 2 | R1 | 0 | 0402 | PANASONIC | ERJ-2GE0R00 | OR EQUIVALENT |
| 9 | 4 | R2, R3, R4, R5 | 0 | 0402 | PANASONIC | ERJ-2GE0R00 | OR EQUIVALENT |
| 10 | 1 | U1 | TRF370333 | QFN_24_163x163_0p50mm | TI | TRF370333 | For TRF370333 EVM, TI supplied |
| | | | TRF370317 | QFN_24_163x163_0p50mm | TI | TRF370317 | For TRF370317 EVM, TI supplied |
| | | | TRF370315 | QFN_24_163x163_0p50mm | TI | TRF370315 | For TRF370315 EVM, TI supplied |
| | | | TRF370417 | QFN_24_163x163_0p50mm | TI | TRF370417 | For TRF370417 EVM, TI supplied |
| 11 | 2 | TP1, TP3 | BLK | TP_THVT_100_RND | KEYSTONE | 5001K | |
| 12 | 2 | TP2, TP4 | RED | TP_THVT_100_RND | KEYSTONE | 5000K | |

3 Circuit Description

This chapter discusses the various functions of the EVM.

3.1 Circuit Function

- Headers TP2 and TP4 supply 5-V V_{CC} dc power to the modulator. Header TP4 supplies 5 V to the LO circuitry, and TP2 supplies 5 V to the modulator circuitry.
- Four SMA connectors are provided on the EVM for inputting differential I/Q signals directly to the input pins of the TRF370x. Connectors J3, J4, J5, and J6 are used to connect the signal source I/Q signals directly to the TRF370x.
- Two SMA connectors are provided for LO input: J1 = LOP and J2 = LON. Terminate whichever LO port is not being used through 50 Ω to ground.
- One SMA connector is for RF_OUT: J7.

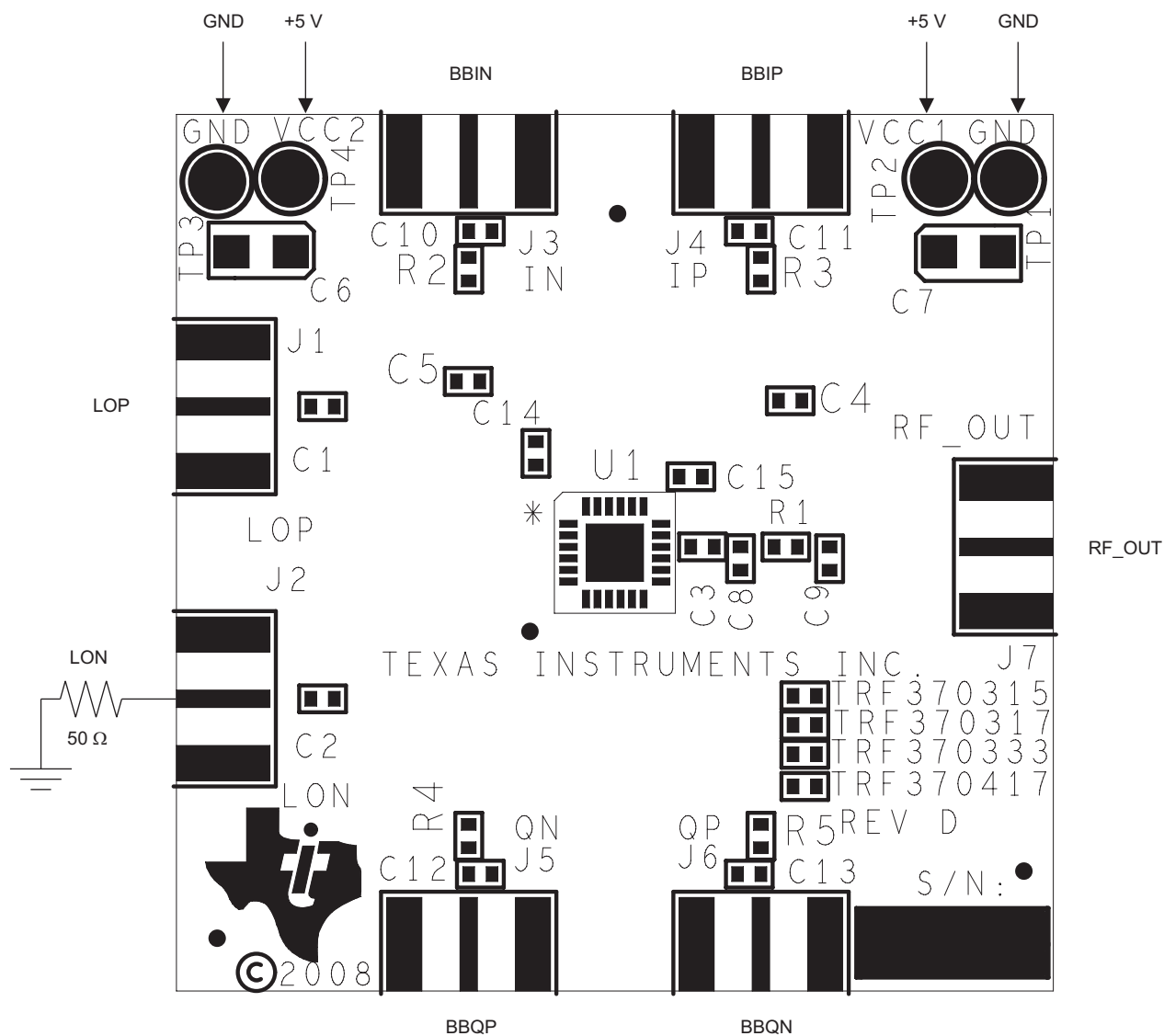
3.1.1 Power

Table 2. Power Supply Connection

| Power Supply Connection | Description |
|-------------------------|------------------------------------|
| TP4 | 5-V (V_{CC}), U1 analog supply |
| TP2 | 5-V (V_{CC}), U1 analog supply |
| TP3, TP1 | Analog ground |

4 Circuit Board

This chapter shows the circuit board test points.



K007

Figure 13. Silkscreen Top Layer

This chapter shows the EVM schematic.



DNI = Do not install.

Figure 14. TRF370x EVM Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4.5 V to 5.5 V and the output voltage range of 4.5 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 59°C. The EVM is designed to operate properly with certain components above -40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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| DLP® Products | www.dlp.com | Communications and Telecom | www.ti.com/communications |
| DSP | dsp.ti.com | Computers and Peripherals | www.ti.com/computers |
| Clocks and Timers | www.ti.com/clocks | Consumer Electronics | www.ti.com/consumer-apps |
| Interface | interface.ti.com | Energy | www.ti.com/energy |
| Logic | logic.ti.com | Industrial | www.ti.com/industrial |
| Power Mgmt | power.ti.com | Medical | www.ti.com/medical |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Space, Avionics & Defense | www.ti.com/space-avionics-defense |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video and Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless-apps |

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